COA — Computer Organization & Architecture

Scanned question papers, topic-wise · Dec 2025 (QP 98169) + May 2026 (QP 09161)

Every question is the original scanned print from the university paper — nothing re-typed.

SOLVING QUESTIONS

Topic-wise · Dec 2025 + May 2026 · 8 questions

Q1 Attempt any THREE

1. Number Conversion — Decimal to Binary / Octal / Hexadecimal

Dec 2025 · Q1A · 5 marks

A Convert the following decimal number to Binary, Octal and Hexadecimal number. 5

a) $(345.35)_{10}$ b) $(818.55)_{10}$

May 2026 · Q1A · 5 marks

A Convert $(74.25)_{10}$ and $(47.50)_{10}$ into hexadecimal numbers and perform addition on converted numbers. 5

2. IEEE 754 Floating-Point Format — Single Precision

May 2026 · Q2a · 8 marks

Q.2 A Convert $(56.45)_{10}$ into IEEE 754 floating point Single Precision format. 8

3. Non-Restoring Division — Flowchart & Implementation

Dec 2025 · Q2a · 8 marks

Q2 A Draw flowchart for non restoring division algorithm and implement for (13/3) 8

May 2026 · Q3a · 8 marks

Q.3 A Draw flow chart for nonrestoring division algorithm and solve $(15)_{10}$ / $(2)_{10}$. 8

4. Cache Address Format — Direct & Associative Mapping

Dec 2025 · Q3a · 8 marks

Q3 A A computer has 64MB main memory and 32KB cache memory. Each line in cache stores 8bytes. 8

Show the format for memory address for Direct and Associative mapping.

5. Booth's Algorithm — Signed Multiplication

Dec 2025 · Q5b · 7 marks

B Multiply $(12)_{10}$ and $(-5)_{10}$ using Booth's algorithm. 7

May 2026 · Q5b · 7 marks

B Multiply $(-8)_{10}$ and $(-3)_{10}$ using Booth's algorithm 7

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THEORY QUESTIONS

Topic-wise · Dec 2025 + May 2026 · 21 questions

Q1 Attempt any THREE

1. 8086 Microprocessor — Architecture & Addressing Modes

Dec 2025 · Q1B · 5 marks

B Explain addressing modes of 8086 with suitable example. 5

Dec 2025 · Q5a · 8 marks

Q5 A Explain with suitable diagram Architecture of 8086 microprocessor. 8

May 2026 · Q5a · 8 marks

Q.5 A Explain architecture of 8086 microprocessor. 8

2. Memory — Hierarchy, Characteristics & Associative Memory

Dec 2025 · Q2b · 7 marks

B Explain memory hierarchy with diagrams and characteristics of memory. 7

May 2026 · Q1C · 5 marks

C Explain characteristics of memory. 5

Dec 2025 · Q1C · 5 marks

C Explain Associative memory with its usages. 5

May 2026 · Q1D · 5 marks

D Explain Associative memory. 5

3. Cache Mapping Techniques — Direct, Associative & Set Associative

May 2026 · Q4a · 8 marks

Q.4 A Compare Direct, Associative, Set Associative Cache Mapping techniques. 8

4. Control Unit Design — Microprogrammed, Hardwired & Microinstruction

Dec 2025 · Q4a · 8 marks

Q4 A Explain micro- programmed control unit with suitable diagram. 8

May 2026 · Q4b · 7 marks

B Compare Hardwired and Softwired control unit design techniques. 7

Dec 2025 · Q6c · 5 marks

C Differentiate horizontal and vertical microinstruction. 5

5. Pipelining & Pipeline Hazards

May 2026 · Q1B · 5 marks

B Explain instruction pipeline. 5

Dec 2025 · Q4b · 7 marks

B Draw and explain the various pipeline hazards and method to resolve it. 7

May 2026 · Q2b · 7 marks

B Explain different pipeline hazards. 7

6. I/O Data Transfer Methods — Programmed, Interrupt-Driven & DMA

Dec 2025 · Q3b · 7 marks

B Explain and compare programmed I/O, interrupt-driven I/O, and DMA. 7

May 2026 · Q3b · 7 marks

B Explain programmed IO and interrupt-driven data transfer methods. 7

7. Buses & Bus Arbitration — ISA, PCI & USB

Dec 2025 · Q1D · 5 marks

D Explain ISA, PCI and USB buses. 5

Dec 2025 · Q6a · 5 marks

Q6 A Explain bus arbitration with examples 5

8. Flynn's Classification

Dec 2025 · Q6b · 5 marks

B Explain Flynn's classification. 5

May 2026 · Q6a · 8 marks

Q.6 A Explain Flynn's classification. 8

9. 80386DX Operation Modes

May 2026 · Q6b · 7 marks

B Differentiate between different operation modes of 80386DX processor 7